Notice of Allowability	Application No.	Applicant(s)	
	10/693,344	KHAN ET AL.	
	Examiner	Art Unit	
	Michael Yaary	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *05/03/2007*.

2. ☒ The allowed claim(s) is/are *1-4,6,8-18,20 and 21*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20070621* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John F. Travis on 06/21/2007.

2. The examiner has amended the claims of the application as follows:

1. An apparatus, comprising:

a first circuitry to permit access, responsive to entering a first password, to a first set of resources to debug a first set of code in memory;

a storage structure to contain a second password;

a second circuitry coupled to the first circuitry and to the storage structure to permit access, responsive to entering the second password, to a second set of resources to debug a second set of code in the memory; wherein said first set of resources comprises a first portion of the memory and said second set of resources comprises a second portion of the memory different than the first portion; and

circuitry to prevent the access responsive to said entering the first password if the access responsive to said entering the second password is enabled, and to prevent the access responsive to said entering the second password if the access responsive to said entering the first password is enabled.

2. The apparatus of claim 1, wherein said access to the second set of resources is through a debug interface.

3. The apparatus of claim 2, adapted to place the second set of code in a substantially different portion of the memory than the first set of code.

4. The apparatus of claim 1, wherein the storage structure comprises a content addressable memory.

5. (Cancelled)

6. The apparatus of claim 1, wherein the storage structure comprises a programmable storage structure.

7. (Cancelled)

8. The apparatus of claim 1, wherein the second set of resources is substantially a subset of the first set of resources.

9. A system, comprising:

a volatile first memory;

a second memory coupled to the first memory to contain code for execution;

a processor coupled to the second memory to execute the code;

a first storage structure coupled to the processor to contain a first password;

a second storage structure coupled to the processor to contain a second password;

circuitry to permit access, responsive to entering the first password, to a first set of resources to debug a first set of code in the second memory, to disable said access to the first set of resources, and to enable access, responsive to entering the second

password, to a second set of resources to debug a second set of code in the second memory; and

wherein said first set of code comprises a first portion of the second memory and said second set of code comprises a second portion of the second memory different than the first portion.

10. The system of claim 9, wherein the first and second access are to be through a debug interface.

11. The system of claim 9, wherein the second storage structure is a content addressable memory.

12. The system of claim 9, wherein the circuitry is adapted to cause the access responsive to said entering the first password and the access responsive to said entering the second password to be mutually exclusive.

13. A method, comprising:

disabling a first password that enables performing a first set of code debug operations;

storing a second password;

entering the second password to enable performing a second set of code debug operations;

wherein being enabled to perform the first set of code debug operations and being enabled to perform the second set of code debug operations are mutually exclusive; and

wherein said first set of code comprises a first portion of memory and said second set of code comprises a second portion of memory different than the first portion.

14. The method of claim 13, wherein said being enabled to perform the second set of code debug operations comprises being enabled to perform a subset of the first code debug operations.

15. The method of claim 13, wherein said first and second code debug operations are performed through a debug interface.

16. The method of claim 13, wherein said disabling the first password results from said storing the second password.

17. The method of claim 13, further comprising enabling a third password that re-enables said performing the first set of code debug operations.

18. A machine-readable storage medium that provides instructions, which when executed by a computing platform, cause said computing platform to perform operations comprising:

receiving a first password to enable debug of a first set of code during a first debug stage;

disabling the first password to prevent further debugging activities during the first debug stage;

storing a second password;

receiving the second password to enable debug of a second set of code during a second debug stage;

wherein the operation of disabling the first password prevents access to the first set of code during the second debug stage; and

wherein said first set of code comprises a first portion of memory and said second set of code comprises a second portion of memory different than the first portion.

19. (Cancelled)

20. The medium of claim 18, wherein the operation of storing the second password results in said disabling the first password.

21. The medium of claim 18, wherein said operations further comprise using a third password to re-enable the debug of the first set of code.

22-35. (Cancelled)

REASONS FOR ALLOWANCE

3. Claims 1-4, 6, 8-18, 20, and 21 are allowed.

4. The following is an examiner's statement of reasons for allowance:

5. The prior art of record fails to teach or suggest the claimed invention. Specifically the prior art of record fails to teach or suggest debugging a first portion of code comprising a first portion of memory and debugging a second set of code comprising a second portion of memory different than the first portion, as recited in independent claims 1, 9, 13, and 18.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Yaary whose telephone number is (571) 270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100